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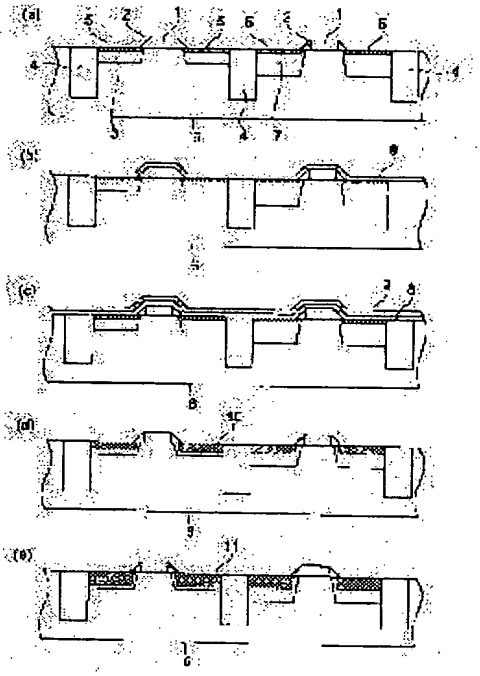
(54) METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To form a homogeneous silicide layer that less produces a defect such as a junction leak.
SOLUTION: A method for manufacturing a semiconductor device includes a preheating step of heating the surface of a silicon layer during formation of a metal film, when the metal film is formed on the silicon layer and then the silicon layer is heated to make the metal film react with the silicon layer and to form the silicide layer on the silicon layer.



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CLAIMS

[Claim(s)]
[Claim 1] The manufacture approach of the semiconductor device which performs 1st heating, carries out the laminating of the metal membrane in the condition, performs 2nd heating on the front face of a silicon layer, and is subsequently characterized by the thing of a silicon layer for which a surface layer is silicide-ized at least on it.
[Claim 2] The manufacture approach of a semiconductor device according to claim 1 that whenever [stoving temperature / of ** a 1st] is 300-400 degrees C.
[Claim 3] The manufacture approach of a semiconductor device according to claim 1 that whenever [stoving temperature / of ** a 2nd] is 500-900 degrees C.
[Claim 4] The manufacture approach of the semiconductor device any one publication of three from claim 1 which forms the antioxidizing film on the surface of a metal membrane, and subsequently performs 2nd heating where the temperature of the front face of a silicon layer is once dropped from whenever [stoving temperature / of ** a 1st] after a metal membrane is formed.
[Claim 5] The manufacture approach of the semiconductor device according to claim 4 which forms the antioxidizing film on the surface of a metal membrane where the temperature of the front face of a silicon layer is once dropped at 200 degrees C or less from whenever [stoving temperature / of ** a 1st].
[Claim 6] The manufacture approach of the semiconductor device any one publication of five from claim 1 which includes the process which makes some or all of a field from the front face of a silicon layer to a depth of 12nm make it amorphous before performing 1st heating.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of the semiconductor device of a silicon layer which silicide-izes a surface layer at least in more detail about the manufacture approach of a semiconductor device.
[0002]
[Description of the Prior Art] Detailed-ization of device size is advanced in manufacture of a semiconductor device. This is for leading to improvement in the property of a transistor, when the number of devices which can be taken from one substrate increases and a semiconductor device contains a transistor so that detailed-ization progresses. However, resistance of the wiring part instead of the transistor itself has come to affect the working speed of a transistor with progress of detailed-izing. For this reason, in manufacture of a semiconductor device, the Salicide technique for lowering resistance of a gate line or a diffusion field is indispensable.
[0003] In manufacture of the semiconductor device using the Salicide technique, the usual transistor production is first performed to a silicon substrate. That is, it is formation of a component isolation region, a well, the gate, and an N+/P+ diffusion layer. Next, after performing surface treatment using a hydrofluoric acid water solution etc. to the silicon substrate which ended the above-mentioned transistor formation process and exposing a silicon front face, a metal membrane is formed on a silicon front face.
[0004] subsequently, the protective coat for preventing oxidation of said metal membrane on this metal membrane -- preparing -- further -- RTA Processing (Rapid Thermal Annealling) etc. -- a substrate is heated (annealing for forming silicide) and a silicide layer is formed on a substrate by making the silicon and said metal membrane of a substrate react. On the front face of a silicon substrate in which the silicide layer was formed, the part which does not cause silicide reactions, such as a component isolation region formed with the oxide film or a sidewall, exists.
[0005] Since these parts are parts for electrical isolation, if the unreacted metal remains on this, they have a problem. Then, drugs processing which removes the unreacted metal membrane on a component isolation region or a sidewall is performed. The drug solution which dissolves said metal membrane formed on the surface of the silicon substrate, and does not dissolve silicide is used for this processing.
[0006] Finally, at temperature higher than whenever [in annealing for forming the aforementioned silicide / stoving temperature], annealing for the phase change of silicide is performed and a silicide layer is changed to the structure where resistance is more low. The reason for dividing annealing treatment into 2 times is because the silicon of a substrate is violently spread into the metal membrane on a component isolation region or a sidewall and silicide is formed also on a component isolation region or a sidewall, when temperature is raised by annealing for forming silicide too much. By using such a Salicide technique, the electric conduction field of low resistance can be produced only on a silicon front face by using the selectivity of a reaction, without using the conventional photolithography technique.
[0007] However, the fault of the approach using the above-mentioned Salicide technique is consuming the silicon of a substrate in the case of formation of silicide. If the thickness of an

N+/P+ diffusion layer turns thinner up with advance of detailed-izing and the silicon of this field is consumed for formation of a silicide layer, the distance for the inferior surface of tongue of the formed silicide layer and the joint under an N+/P+ diffusion layer will approach further, and it will become easy to produce junction leak. In this case, although consumption of the silicon at the time of formation of silicide is held down, the distance of a part for said joint and the base of a silicide layer becomes large and junction leak can be reduced if a silicide layer is made thin, the rise of the sheet resistance of a gate line or a diffusion field is caused inevitably.

[0008] Usually, the technique of forming silicide evenly is used as a cure for suppressing junction leak and the rise of sheet resistance. It is known that the surface smoothness of silicide will change to the reaction time of the above metals and silicon a lot based on the condition on the front face of silicon of a substrate. This is to put a silicon front face to atmospheric air, by the time it forms a metal membrane, even if it removes an oxide film from the front face of the silicon of a substrate by pretreatment etc., and for an oxide film to arise again.

[0009] Silicide will be formed if it is the case that a metal membrane and the oxide film produced between substrate silicon are very thin. This is because there is usually reducibility to silicon oxide in the metal used for formation of silicide. However, the part which silicide tends to produce since it is usually uneven, and the part which is hard to produce are formed, and, as for the oxide film produced on the surface of a silicon substrate, a silicide layer uneven as a result is formed on a silicon substrate. In order that the distance for the base of a silicide layer and the joint under an N+/P+ diffusion layer may approach in a part with the thick thickness, a lifting and since [which become empty] the average thickness of the silicide layer itself is still thinner, the silicide layer formed on the uneven oxide film has large sheet resistance in junction leak.

[0010] Moreover, depending on a device, carbon, a fluorine, etc. may mix in a silicon front face in the middle of the making process. In the process of gate etching, the etchback at the time of sidewall formation, etc., it is mainly easy to produce these. Mixing of such an element increases the heterogeneity on the front face of silicon, and is considered to produce junction leak according to the same operation as the heterogeneity by the above mentioned oxide film.

[0011] The heterogeneity of such silicide is improved and there is the manufacture approach of the semiconductor device indicated by for example, the publication-number No. 251967 [nine to] official report as an approach of preventing junction leak. The manufacture approach indicated by the above-mentioned official report is explained in order of a process, referring to drawing 2 . In addition, since this drawing is a schematic diagram to which the scale was expanded partially because of explanation, that configuration or magnitude of it is not necessarily the same as that of an actual device.

[0012] (a) of drawing 2 After ending formation of a transistor, it is in the condition which made the silicon front face amorphous. A diffusion layer with deep amorphous field in which the gate, a diffusion layer with 102 [shallow / a sidewall and 103], and 104 were formed in of the component isolation region, and 105 was formed for 101 of impregnation of ion and 107, and 106 are silicon (silicon wafer) as a substrate. In order to simplify explanation, gate oxide, a well, etc. are omitted all over drawing.

[0013] (b) of drawing 2 It is in the condition which ended formation of a metal membrane 108 and the antioxidizing film 109. Cobalt is well used for a metal membrane 108, and cobalt reacts to it with silicon 106, and it is made to produce silicide. Titanium nitride is well used for the antioxidizing film 109, and functions on it as film which prevents oxidation of a metal membrane 108.

[0014] (c) of drawing 2 The aforementioned (b) It is a condition and is in the condition after performing annealing which forms silicide. The silicide layer 110 is the aforementioned (a). It is formed so that it may be settled in the amorphous field 105 set and prepared. In order that the silicon in the amorphous field 105 made amorphous to homogeneity and the cobalt of a metal membrane 109 may react, the formed silicide layer 110 has high surface smoothness. (d) of drawing 2 (c) It is a condition and is in the condition after performing annealing for the phase change of silicide. Annealing for the phase change of silicide is performed at an elevated temperature rather than annealing which forms silicide. By this annealing treatment, it is (c). The produced silicide layer 110 reacts with the silicon 106 of a substrate further, and the silicide

layer 111 in which thickness increased is formed. In addition, the aforementioned (c) Since it sets and the uniform silicide layer 110 arises, the distance of extent from which the distance of the PN-junction section and the silicide layer 110 does not produce junction leak in the nearest part in this condition is maintained.

[0015]

[Problem(s) to be Solved by the Invention] As described above, in order to pour in ion and to perform amorphous-ization on the front face of silicon, ion, such as arsenic with comparatively large mass, is usually used. However, while such ion tends to form an amorphous layer, it is known that it will be easy to produce a defect to a field deeper than the field where ion was poured in. If such a defect arises, it will be easy to produce the level constituting the cause of junction leak of silicon. Increase of leakage current is LSI for pocket devices which increases the consumed electric current at the time of standby of a component, and especially operates by a cell etc. It sets and becomes a serious problem.

[0016] This invention is made in view of the above-mentioned trouble, and it is more uniform and aims at forming in a semiconductor device the silicide layer which cannot produce defects, such as junction leak, easily.

[0017]

[Means for Solving the Problem] According to this invention, the manufacture approach of the semiconductor device which performs 1st heating on the front face of a silicon layer, carries out the laminating of the metal membrane in that condition to it, subsequently performs 2nd heating on it, and is characterized by the thing of a silicon layer for which a surface layer is silicide-ized at least on it is offered.

[0018] That is, in this invention, in order to form the oxide film and metal membrane which are formed in the front face of a silicon layer using the heat energy which the front face of the silicon layer by which the temperature up was carried out has, the metal atom supplied to the front face of a silicon layer is made to react, and said oxide film is returned. this -- said oxide film -- disappearance -- or since it thin-film-izes, a uniform and flat silicide layer can be formed in the front face of a silicon layer.

[0019] As a silicon layer in this invention, the silicon substrate itself in which the circuit section of semiconductor devices, such as a capacitor and a transistor, is formed is sufficient, and the silicon layer which functions as the conductive layer or wiring layer of these components is sufficient.

[0020] Whenever [stoving temperature / of ** a 1st] has desirable 300-400 degrees C. If whenever [stoving temperature / of ** a 1st] is lower than 300 degrees C, it will be easy to produce irregularity in the interface of silicon and a silicide layer. If whenever [stoving temperature / of ** a 1st] is higher than 400 degrees C, it will be easy to produce proof-pressure degradation of gate oxide etc. by the plasma damage during the spatter of a metal membrane.

[0021] Although refractory metals, such as cobalt and titanium, are mentioned, if it is the metal which reacts with silicon and forms silicide as an ingredient of the metal membrane in this invention, it will not be limited especially. As the formation approach of a metal membrane, the conventional thin film coating technology, such as vacuum deposition, a CVD method, and a spatter, can be used.

[0022] As a means of the 2nd heating, annealing by furnace annealing, RTA, etc. in this invention is mentioned. Whenever [stoving temperature / of ** a 2nd] has desirable 500-900 degrees C.

[0023] After a metal membrane is formed, where the temperature of the front face of a silicon layer is once dropped from whenever [stoving temperature / of ** a 1st], the antioxidizing film is formed in this invention on the surface of a metal membrane, and, subsequently the process which performs 2nd heating is included in it. That is, since the amount of currents which flows the inside of an oxide film during membrane formation of a metal membrane can be reduced by the above-mentioned cooling although pressure-proofing of gate oxide may be degraded when silicide-izing the silicon layer which constitutes a transistor using the manufacture approach including the 1st heating process of this invention, pressure-proof degradation of the above is prevented. That the temperature of the silicon layer at the time of antioxidizing film formation

should just be descending at 200 degrees C or less, especially a minimum may not set and may be cooled to near a room temperature. As an ingredient of the antioxidizing film in this invention, although titanium nitride is mentioned, if it is the ingredient of the conventional antioxidizing film, it will not be limited especially. As the formation approach of the antioxidizing film, the conventional thin film coating technology, such as vacuum deposition, a CVD method, and a spatter, can be used. In this invention, since the membrane formation equipment used for formation of a metal membrane can perform formation of the antioxidizing film continuously, oxidation of a metal membrane can be prevented.

[0024] After using the above-mentioned approach, when asking for the improvement of the further junction leak, before performing 1st heating, it is desirable to make some or all of a field from the front face of a silicon layer to a depth of 12nm make it amorphous. That is, since the front face of a silicon layer is polluted with carbon, a fluorine, etc., even if it makes temperature of a silicon layer high and forms a metal, when the silicide formed becomes an ununiformity, by making the maximum front face of a silicon layer amorphous, association of carbon, a fluorine, and silicon is cut and a reaction with said metal is promoted. The reaction of said metal and silicon comes to progress to homogeneity by this, silicide is formed in homogeneity, and junction leak is controlled. As for the above-mentioned amorphous-izing, it is desirable to be carried out so that an ion kind may be spread only into a part shallow in the management of a silicon layer and an ion kind may not usually invade into a part with a deep silicon layer.

[0025] It mainly depends for the penetration depth of an ion kind on impregnation energy. Boron, phosphorus, arsenic, nitrogen, silicon, etc. are mentioned as an ion kind used for the above-mentioned shallow ion implantation. Also in these, comparatively heavy arsenic is desirable. The ion injection rate in this invention is one E14 to 8E14-/cm2 order, and ion-implantation energy is 5-15keV. Although illustrated, these are suitably adjusted according to the purpose.

[0026] As mentioned above, even if the field which produces a defect with the ion kind poured in since it was small compared with the former occurs in a silicon layer, since that depth is not not much deep, the ion-implantation energy in this invention does not affect a junction field.

[0027] By this invention, in the condition that the front face of a silicon layer is not exposed, an ion implantation can be performed (for example, where it is in a condition [not continuing not removing the oxide film which exists in a silicon front face] or the laminating of the protective coat is carried out), and an ion kind can be injected only into the shallow part of the management of a stop and a silicon layer for invasion of the ion kind to a part with a silicon layer deep as a result. Therefore, with respect to the capacity of ion implantation equipment, a shallow ion implantation [be / nothing] becomes possible.

[0028]

[Embodiment of the Invention] Hereafter, this invention is not limited by these although the gestalt of implementation of the manufacture approach of the semiconductor device of this invention is explained based on a drawing. Drawing 1 shows the outline of the production process of the MOS transistor by this invention. In addition, since drawing 1 has expanded the scale partially because of explanation, it is not necessarily the same as the configuration of an actual device. Moreover, gate oxide, a well, etc. are omitting out of drawing for simplification.

[0029] The example of this invention is explained referring to example drawing 1 . (a) of drawing 1 After ending formation of a MOS transistor, the condition of having made the silicon front face amorphous is shown. As for a gate electrode, a diffusion layer with 2 [shallow / a sidewall and 3], and 4, 1 is [a component isolation region, a diffusion layer with 5 / deep / an amorphous layer and 7 /, and 6] silicon substrates (silicon wafer).

[0030] Formation of an amorphous layer is performed when contamination of carbon, a fluorine, etc. has arisen on the front face of the silicide-ized silicon substrate 6. The depth of 120nm and the deep diffusion layer 7 of the depth of the shallow diffusion layer 3 is 160nm. Each of diffusion layers 3 and 7 is BF2. And it is produced by impregnation of As.

[0031] Formation of a sidewall 2 has a method of leaving an about 10nm oxide film in the front face of the approach of carrying out etchback to the front face of a silicon substrate 6, and silicon 6. According to the latter approach, contamination of the carbon under the effect of etching produced on the front face of a silicon substrate 6 or a fluorine can be reduced, but it

may be difficult for the thickness which should be carried out etchback to change with parts, and to leave an oxide film to the front face of silicon 6 in the case where two or more devices are produced in the same process.

[0032] Impregnation of arsenic ion performed formation of the amorphous layer 5. Usually, if arsenic ion is injected into a silicon substrate 6, an amorphous field will be produced in the front-face side of a silicon substrate 6 rather than average projection range. In a part still deeper than average projection range, the field which Si atom begun to beat by poured-in As entered is produced. A defect tends to be made in such a field and a rearrangement is further produced according to a heating process. It becomes the cause in which these produce junction leak.

[0033] However, in order to pour arsenic ion into the very shallow field of the front face of a silicon substrate 6 in this invention, 10keV(s) and the amount of impregnation ion of impregnation energy (the amount of dopes) are 3E14/cm2. Thus, since impregnation energy is small, even if the field which the silicon atom begun to beat with the arsenic ion poured in as described above entered is generated, since the depth is not not much deep, a junction field is not affected.

[0034] (b) of drawing 1 It is in the condition which ended formation of a metal membrane 8 after the 1st heating. A metal membrane 8 is a metal membrane for reacting with a silicon substrate 6 and producing silicide, and cobalt was used for it in this example. The spatter performed membrane formation of a metal membrane 8. They are 5mT(s) about the pressure in 500W and equipment in the power of a sputtering system. It considered as extent. Temperature (whenever [stoving temperature / of ** a 1st]) of the silicon substrate 6 at the time of a spatter was made into 350 degrees C. In addition, below 300 degrees C, irregularity arises in the interface of silicide and silicon and whenever [stoving temperature / of ** a 1st] tends to produce junction leak by it. In order to reduce junction leak, sheet resistance will become high, if irregularity is left as it is and a metal membrane 8 is made thin. Above 400 degrees C, gate oxide produces [whenever / stoving temperature / of ** a 1st] proof-pressure degradation by the plasma damage during a spatter.

[0035] (c) of drawing 1 It is in the condition which the temperature of a silicon substrate 6 was once dropped after formation termination of a metal membrane 8, and formed the antioxidizing film 9 in the condition. The antioxidizing film 9 formed membranes by the spatter using titanium nitride in this example. They are 10mT(s) about the pressure in 2kW and equipment in the power of a sputtering system. It considered as extent. The spatter of a metal membrane 8 and the spatter of the antioxidizing film 9 were performed continuously, maintaining a vacuum within the same sputtering system. This is for preventing oxidation of the cobalt of a metal membrane 8. In addition, the temperature of the silicon substrate 6 at the time of spatter initiation was 70 degrees C.

[0036] If the temperature of a silicon substrate 6 exceeds 200 degrees C at the time of the spatter of the antioxidizing film 9, pressure-proofing of gate dielectric film may deteriorate by the damage of the plasma at the time of the spatter of the antioxidizing film 9. The degree of pressure-proof degradation changes with devices. When degradation of pressure-proofing of gate dielectric film was checked, the temperature of a silicon substrate 6 was lowered to 200 degrees C, holding a silicon substrate 6, where the vacuum of E-108 order is maintained in the same equipment after the spatter of a metal membrane 8. However, in order to lower substrate temperature to 200 degrees C, the processing time becomes long, and a throughput falls.

[0037] (d) of drawing 1 After ending formation of the antioxidizing film 9, it is in the condition after performing 2nd heat-treatment. The silicide layer 10 is formed in diffusion layers 3 and 7, respectively. Whenever [stoving temperature / of ** a 2nd] was 570 degrees C. Drawing 1 (e) is the above (d). It is in the condition which heat-treated high temperature further from the condition. By heat-treatment of high temperature, it is the above (d). It became the silicide layer 11 in which the produced silicide layer 10 reacted to with the silicon substrate 6 further, and thickness increased.

[0038] [Example of a comparison] N+ of the device used as a sample It is As to a diffusion layer field 50keV(s) and 3E15/cm 2 It is conditions and is P+. He is BF2 to a diffusion layer field. 30keV(s) and 2E15cm2 After pouring in on conditions, it is RTA for 10 seconds at 1000 degrees

C. Annealing was performed. Then, 20keV and 3E14/cm 2 As was poured in on the surface of the silicon substrate on conditions. This process is an approach by the conventional technique which makes Si amorphous.
[0039] Then, HF water solution removed the natural oxidation film of a silicon substrate surface. Subsequently it is TiN in 80A of thickness about Co. By thickness 200 **, membranes are formed by the continuation spatter in a vacuum in this order, respectively, and it is RTA. 570 degrees C and annealing for 60 seconds which were used were performed in nitrogen-gas-atmosphere mind. Subsequently, a sulfuric-acid:filtered water = Co and TiN unreacted with the solution of 4:1 It removed. At this time, the thickness of silicide was about 150 **. Then, it is RTA about annealing for 30 seconds at 750 **. It was used and carried out in nitrogen-gas-atmosphere mind. The final thickness of a silicide layer was about 300 **.
[0040] Average junction leakage current was 1.8V, and the samples in which the silicide layer was formed by the conventional approach were 1.8E-8A/cm2 (N+ diffusion layer side) and 3.4E-7A/cm2 (P+ diffusion layer side). On the other hand, average junction leakage current was 1.8V, and the samples in which silicide was formed with the application of the manufacture approach of the semiconductor device of this invention shown in said example were 1.8E-8A/cm2 (N+ diffusion layer side) and 2.5E-8A/cm2 (P+ diffusion layer side). Leakage current is 1 although the junction to a part for the joint under an N+/P+ diffusion layer is not destroyed in the sample devices in which the silicide layer was formed by the conventional approach. It increased double figures from the digit.
[0041]
[Effect of the Invention] In this invention, in order to form the oxide film and metal membrane which are formed in the front face of a silicon layer using the heat energy which the front face of the silicon layer by which the temperature up was carried out has, the metal atom supplied to the front face of a silicon layer is made to react, and said oxide film is returned. this -- said oxide film -- disappearance -- or since it thin-film-izes, a uniform and flat silicide layer can be formed in the front face of a silicon layer. Therefore, it is hard coming to generate the junction leak in a semiconductor device. Moreover, after forming a metal membrane, degradation of the pressure-proofing in the semiconductor device formed in a silicon layer is prevented by forming the antioxidizing film, where the temperature of a silicon layer is once dropped.
[0042] By making the front face of a silicon layer amorphous, association of carbon, a fluorine, and silicon is cut and the reaction of the metal atom and silicon which form a metal membrane is promoted. By this, the reaction of a metal membrane and silicon progresses to homogeneity, silicide is formed in homogeneity, and junction leak is controlled.

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the manufacture approach of the semiconductor device of a silicon layer which silicide-izes a surface layer at least in more detail about the manufacture approach of a semiconductor device.

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PRIOR ART

[Description of the Prior Art] Detailed-ization of device size is advanced in manufacture of a semiconductor device. This is for leading to improvement in the property of a transistor, when the number of devices which can be taken from one substrate increases and a semiconductor device contains a transistor so that detailed-ization progresses. However, resistance of the wiring part instead of the transistor itself has come to affect the working speed of a transistor with progress of detailed-izing. For this reason, in manufacture of a semiconductor device, the Salicide technique for lowering resistance of a gate line or a diffusion field is indispensable.
[0003] In manufacture of the semiconductor device using the Salicide technique, the usual transistor production is first performed to a silicon substrate. That is, it is formation of a component isolation region, a well, the gate, and an N+/P+ diffusion layer. Next, after performing surface treatment using a hydrofluoric acid water solution etc. to the silicon substrate which ended the above-mentioned transistor formation process and exposing a silicon front face, a metal membrane is formed on a silicon front face.
[0004] subsequently, the protective coat for preventing oxidation of said metal membrane on this metal membrane -- preparing -- further -- RTA Processing (Rapid Thermal Annealling) etc. -- a substrate is heated (annealing for forming silicide) and a silicide layer is formed on a substrate by making the silicon and said metal membrane of a substrate react. On the front face of a silicon substrate in which the silicide layer was formed, the part which does not cause silicide reactions, such as a component isolation region formed with the oxide film or a sidewall, exists.
[0005] Since these parts are parts for electrical isolation, if the unreacted metal remains on this, they have a problem. Then, drugs processing which removes the unreacted metal membrane on a component isolation region or a sidewall is performed. The drug solution which dissolves said metal membrane formed on the surface of the silicon substrate, and does not dissolve silicide is used for this processing.
[0006] Finally, at temperature higher than whenever [in annealing for forming the aforementioned silicide / stoving temperature], annealing for the phase change of silicide is performed and a silicide layer is changed to the structure where resistance is more low. The reason for dividing annealing treatment into 2 times is because the silicon of a substrate is violently spread into the metal membrane on a component isolation region or a sidewall and silicide is formed also on a component isolation region or a sidewall, when temperature is raised by annealing for forming silicide too much. By using such a Salicide technique, the electric conduction field of low resistance can be produced only on a silicon front face by using the selectivity of a reaction, without using the conventional photolithography technique.
[0007] However, the fault of the approach using the above-mentioned Salicide technique is consuming the silicon of a substrate in the case of formation of silicide. If the thickness of an N+/P+ diffusion layer turns thinner up with advance of detailed-izing and the silicon of this field is consumed for formation of a silicide layer, the distance for the inferior surface of tongue of the formed silicide layer and the joint under an N+/P+ diffusion layer will approach further, and it will become easy to produce junction leak. In this case, although consumption of the silicon at the time of formation of silicide is held down, the distance of a part for said joint and the base of a silicide layer becomes large and junction leak can be reduced if a silicide layer is made thin, the

rise of the sheet resistance of a gate line or a diffusion field is caused inevitably.
[0008] Usually, the technique of forming silicide evenly is used as a cure for suppressing junction leak and the rise of sheet resistance. It is known that the surface smoothness of silicide will change to the reaction time of the above metals and silicon a lot based on the condition on the front face of silicon of a substrate. This is to put a silicon front face to atmospheric air, by the time it forms a metal membrane, even if it removes an oxide film from the front face of the silicon of a substrate by pretreatment etc., and for an oxide film to arise again.
[0009] Silicide will be formed if it is the case that a metal membrane and the oxide film produced between substrate silicon are very thin. This is because there is usually reducibility to silicon oxide in the metal used for formation of silicide. However, the part which silicide tends to produce since it is usually uneven, and the part which is hard to produce are formed, and, as for the oxide film produced on the surface of a silicon substrate, a silicide layer uneven as a result is formed on a silicon substrate. In order that the distance for the base of a silicide layer and the joint under an N+/P+ diffusion layer may approach in a part with the thick thickness, a lifting and since [which become empty] the average thickness of the silicide layer itself is still thinner, the silicide layer formed on the uneven oxide film has large sheet resistance in junction leak.
[0010] Moreover, depending on a device, carbon, a fluorine, etc. may mix in a silicon front face in the middle of the making process. In the process of gate etching, the etchback at the time of sidewall formation, etc., it is mainly easy to produce these. Mixing of such an element increases the heterogeneity on the front face of silicon, and is considered to produce junction leak according to the same operation as the heterogeneity by the above mentioned oxide film.
[0011] The heterogeneity of such silicide is improved and there is the manufacture approach of the semiconductor device indicated by for example, the publication-number No. 251967 [nine to] official report as an approach of preventing junction leak. The manufacture approach indicated by the above-mentioned official report is explained in order of a process, referring to drawing 2 . In addition, since this drawing is a schematic diagram to which the scale was expanded partially because of explanation, that configuration or magnitude of it is not necessarily the same as that of an actual device.
[0012] (a) of drawing 2 After ending formation of a transistor, it is in the condition which made the silicon front face amorphous. A diffusion layer with deep amorphous field in which the gate, a diffusion layer with 102 [shallow / a sidewall and 103], and 104 were formed in of the component isolation region, and 105 was formed for 101 of impregnation of ion and 107, and 106 are silicon (silicon wafer) as a substrate. In order to simplify explanation, gate oxide, a well, etc. are omitted all over drawing.
[0013] (b) of drawing 2 It is in the condition which ended formation of a metal membrane 108 and the antioxidizing film 109. Cobalt is well used for a metal membrane 108, and cobalt reacts to it with silicon 106, and it is made to produce silicide. Titanium nitride is well used for the antioxidizing film 109, and functions on it as film which prevents oxidation of a metal membrane 108.
[0014] (c) of drawing 2 The aforementioned (b) It is a condition and is in the condition after performing annealing which forms silicide. The silicide layer 110 is the aforementioned (a). It is formed so that it may be settled in the amorphous field 105 set and prepared. In order that the silicon in the amorphous field 105 made amorphous to homogeneity and the cobalt of a metal membrane 109 may react, the formed silicide layer 110 has high surface smoothness. (d) of drawing 2 (c) It is a condition and is in the condition after performing annealing for the phase change of silicide. Annealing for the phase change of silicide is performed at an elevated temperature rather than annealing which forms silicide. By this annealing treatment, it is (c). The produced silicide layer 110 reacts with the silicon 106 of a substrate further, and the silicide layer 111 in which thickness increased is formed. In addition, the aforementioned (c) Since it sets and the uniform silicide layer 110 arises, the distance of extent from which the distance of the PN-junction section and the silicide layer 110 does not produce junction leak in the nearest part in this condition is maintained.

[Translation done.]

* NOTICES *

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EFFECT OF THE INVENTION

[Effect of the Invention] In this invention, in order to form the oxide film and metal membrane which are formed in the front face of a silicon layer using the heat energy which the front face of the silicon layer by which the temperature up was carried out has, the metal atom supplied to the front face of a silicon layer is made to react, and said oxide film is returned. this -- said oxide film -- disappearance -- or since it thin-film-izes, a uniform and flat silicide layer can be formed in the front face of a silicon layer. Therefore, it is hard coming to generate the junction leak in a semiconductor device. Moreover, after forming a metal membrane, degradation of the pressure-proofing in the semiconductor device formed in a silicon layer is prevented by forming the antioxidizing film, where the temperature of a silicon layer is once dropped.
[0042] By making the front face of a silicon layer amorphous, association of carbon, a fluorine, and silicon is cut and the reaction of the metal atom and silicon which form a metal membrane is promoted. By this, the reaction of a metal membrane and silicon progresses to homogeneity, silicide is formed in homogeneity, and junction leak is controlled.

[Translation done.]

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] As described above, in order to pour in ion and to perform amorphous-ization on the front face of silicon, ion, such as arsenic with comparatively large mass, is usually used. However, while such ion tends to form an amorphous layer, it is known that it will be easy to produce a defect to a field deeper than the field where ion was poured in. If such a defect arises, it will be easy to produce the level constituting the cause of junction leak of silicon. Increase of leakage current is LSI for pocket devices which increases the consumed electric current at the time of standby of a component, and especially operates by a cell etc. It sets and becomes a serious problem.
[0016] This invention is made in view of the above-mentioned trouble, and it is more uniform and aims at forming in a semiconductor device the silicide layer which cannot produce defects, such as junction leak, easily.

[Translation done.]

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MEANS

[Means for Solving the Problem] According to this invention, the manufacture approach of the semiconductor device which performs 1st heating on the front face of a silicon layer, carries out the laminating of the metal membrane in that condition to it, subsequently performs 2nd heating on it, and is characterized by the thing of a silicon layer for which a surface layer is silicide-ized at least on it is offered.
[0018] That is, in this invention, in order to form the oxide film and metal membrane which are formed in the front face of a silicon layer using the heat energy which the front face of the silicon layer by which the temperature up was carried out has, the metal atom supplied to the front face of a silicon layer is made to react, and said oxide film is returned. this -- said oxide film -- disappearance -- or since it thin-film-izes, a uniform and flat silicide layer can be formed in the front face of a silicon layer.
[0019] As a silicon layer in this invention, the silicon substrate itself in which the circuit section of semiconductor devices, such as a capacitor and a transistor, is formed is sufficient, and the silicon layer which functions as the conductive layer or wiring layer of these components is sufficient.
[0020] Whenever [stoving temperature / of ** a 1st] has desirable 300-400 degrees C. If whenever [stoving temperature / of ** a 1st] is lower than 300 degrees C, it will be easy to produce irregularity in the interface of silicon and a silicide layer. If whenever [stoving temperature / of ** a 1st] is higher than 400 degrees C, it will be easy to produce proof-pressure degradation of gate oxide etc. by the plasma damage during the spatter of a metal membrane.
[0021] Although refractory metals, such as cobalt and titanium, are mentioned, if it is the metal which reacts with silicon and forms silicide as an ingredient of the metal membrane in this invention, it will not be limited especially. As the formation approach of a metal membrane, the conventional thin film coating technology, such as vacuum deposition, a CVD method, and a spatter, can be used.
[0022] As a means of the 2nd heating, annealing by furnace annealing, RTA, etc. in this invention is mentioned. Whenever [stoving temperature / of ** a 2nd] has desirable 500-900 degrees C.
[0023] After a metal membrane is formed, where the temperature of the front face of a silicon layer is once dropped from whenever [stoving temperature / of ** a 1st], the antioxidizing film is formed in this invention on the surface of a metal membrane, and, subsequently the process which performs 2nd heating is included in it. That is, since the amount of currents which flows the inside of an oxide film during membrane formation of a metal membrane can be reduced by the above-mentioned cooling although pressure-proofing of gate oxide may be degraded when silicide-izing the silicon layer which constitutes a transistor using the manufacture approach including the 1st heating process of this invention, pressure-proof degradation of the above is prevented. That the temperature of the silicon layer at the time of antioxidizing film formation should just be descending at 200 degrees C or less, especially a minimum may not set and may be cooled to near a room temperature. As an ingredient of the antioxidizing film in this invention, although titanium nitride is mentioned, if it is the ingredient of the conventional antioxidizing film, it will not be limited especially. As the formation approach of the antioxidizing film, the

conventional thin film coating technology, such as vacuum deposition, a CVD method, and a spatter, can be used. In this invention, since the membrane formation equipment used for formation of a metal membrane can perform formation of the antioxidizing film continuously, oxidation of a metal membrane can be prevented.

[0024] After using the above-mentioned approach, when asking for the improvement of the further junction leak, before performing 1st heating, it is desirable to make some or all of a field from the front face of a silicon layer to a depth of 12nm make it amorphous. That is, since the front face of a silicon layer is polluted with carbon, a fluorine, etc., even if it makes temperature of a silicon layer high and forms a metal, when the silicide formed becomes an ununiformity, by making the maximum front face of a silicon layer amorphous, association of carbon, a fluorine, and silicon is cut and a reaction with said metal is promoted. The reaction of said metal and silicon comes to progress to homogeneity by this, silicide is formed in homogeneity, and junction leak is controlled. As for the above-mentioned amorphous-izing, it is desirable to be carried out so that an ion kind may be spread only into a part shallow in the management of a silicon layer and an ion kind may not usually invade into a part with a deep silicon layer.

[0025] It mainly depends for the penetration depth of an ion kind on impregnation energy. Boron, phosphorus, arsenic, nitrogen, silicon, etc. are mentioned as an ion kind used for the above-mentioned shallow ion implantation. Also in these, comparatively heavy arsenic is desirable. The ion injection rate in this invention is one E14 to 8E14-/cm2 order, and ion-implantation energy is 5-15keV. Although illustrated, these are suitably adjusted according to the purpose.

[0026] As mentioned above, even if the field which produces a defect with the ion kind poured in since it was small compared with the former occurs in a silicon layer, since that depth is not not much deep, the ion-implantation energy in this invention does not affect a junction field.

[0027] By this invention, in the condition that the front face of a silicon layer is not exposed, an ion implantation can be performed (for example, where it is in a condition [not continuing not removing the oxide film which exists in a silicon front face] or the laminating of the protective coat is carried out), and an ion kind can be injected only into the shallow part of the management of a stop and a silicon layer for invasion of the ion kind to a part with a silicon layer deep as a result. Therefore, with respect to the capacity of ion implantation equipment, a shallow ion implantation [be / nothing] becomes possible.

[0028]

[Embodiment of the Invention] Hereafter, this invention is not limited by these although the gestalt of implementation of the manufacture approach of the semiconductor device of this invention is explained based on a drawing. Drawing 1 shows the outline of the production process of the MOS transistor by this invention. In addition, since drawing 1 has expanded the scale partially because of explanation, it is not necessarily the same as the configuration of an actual device. Moreover, gate oxide, a well, etc. are omitting out of drawing for simplification.

[0029] The example of this invention is explained referring to example drawing 1 . (a) of drawing 1 After ending formation of a MOS transistor, the condition of having made the silicon front face amorphous is shown. As for a gate electrode, a diffusion layer with 2 [shallow / a sidewall and 3], and 4, 1 is [a component isolation region, a diffusion layer with 5 / deep / an amorphous layer and 7 /, and 6] silicon substrates (silicon wafer).

[0030] Formation of an amorphous layer is performed when contamination of carbon, a fluorine, etc. has arisen on the front face of the silicide-ized silicon substrate 6. The depth of 120nm and the deep diffusion layer 7 of the depth of the shallow diffusion layer 3 is 160nm. Each of diffusion layers 3 and 7 is BF2. And it is produced by impregnation of As.

[0031] Formation of a sidewall 2 has a method of leaving an about 10nm oxide film in the front face of the approach of carrying out etchback to the front face of a silicon substrate 6, and silicon 6. According to the latter approach, contamination of the carbon under the effect of etching produced on the front face of a silicon substrate 6 or a fluorine can be reduced, but it may be difficult for the thickness which should be carried out etchback to change with parts, and to leave an oxide film to the front face of silicon 6 in the case where two or more devices are produced in the same process.

[0032] Impregnation of arsenic ion performed formation of the amorphous layer 5. Usually, if

arsenic ion is injected into a silicon substrate 6, an amorphous field will be produced in the front-face side of a silicon substrate 6 rather than average projection range. In a part still deeper than average projection range, the field which Si atom begun to beat by poured-in As entered is produced. A defect tends to be made in such a field and a rearrangement is further produced according to a heating process. It becomes the cause in which these produce junction leak.

[0033] However, in order to pour arsenic ion into the very shallow field of the front face of a silicon substrate 6 in this invention, 10keV(s) and the amount of impregnation ion of impregnation energy (the amount of dopes) are 3E14/cm2. Thus, since impregnation energy is small, even if the field which the silicon atom begun to beat with the arsenic ion poured in as described above entered is generated, since the depth is not not much deep, a junction field is not affected.

[0034] (b) of drawing 1 It is in the condition which ended formation of a metal membrane 8 after the 1st heating. A metal membrane 8 is a metal membrane for reacting with a silicon substrate 6 and producing silicide, and cobalt was used for it in this example. The spatter performed membrane formation of a metal membrane 8. They are 5mT(s) about the pressure in 500W and equipment in the power of a sputtering system. It considered as extent. Temperature (whenever [stoving temperature / of ** a 1st]) of the silicon substrate 6 at the time of a spatter was made into 350 degrees C. In addition, below 300 degrees C, irregularity arises in the interface of silicide and silicon and whenever [stoving temperature / of ** a 1st] tends to produce junction leak by it. In order to reduce junction leak, sheet resistance will become high, if irregularity is left as it is and a metal membrane 8 is made thin. Above 400 degrees C, gate oxide produces [whenever / stoving temperature / of ** a 1st] proof-pressure degradation by the plasma damage during a spatter.

[0035] (c) of drawing 1 It is in the condition which the temperature of a silicon substrate 6 was once dropped after formation termination of a metal membrane 8, and formed the antioxidizing film 9 in the condition. The antioxidizing film 9 formed membranes by the spatter using titanium nitride in this example. They are 10mT(s) about the pressure in 2kW and equipment in the power of a sputtering system. It considered as extent. The spatter of a metal membrane 8 and the spatter of the antioxidizing film 9 were performed continuously, maintaining a vacuum within the same sputtering system. This is for preventing oxidation of the cobalt of a metal membrane 8. In addition, the temperature of the silicon substrate 6 at the time of spatter initiation was 70 degrees C.

[0036] If the temperature of a silicon substrate 6 exceeds 200 degrees C at the time of the spatter of the antioxidizing film 9, pressure-proofing of gate dielectric film may deteriorate by the damage of the plasma at the time of the spatter of the antioxidizing film 9. The degree of pressure-proof degradation changes with devices. When degradation of pressure-proofing of gate dielectric film was checked, the temperature of a silicon substrate 6 was lowered to 200 degrees C, holding a silicon substrate 6, where the vacuum of E-108 order is maintained in the same equipment after the spatter of a metal membrane 8. However, in order to lower substrate temperature to 200 degrees C, the processing time becomes long, and a throughput falls.

[0037] (d) of drawing 1 After ending formation of the antioxidizing film 9, it is in the condition after performing 2nd heat-treatment. The silicide layer 10 is formed in diffusion layers 3 and 7, respectively. Whenever [stoving temperature / of ** a 2nd] was 570 degrees C. Drawing 1 (e) is the above (d). It is in the condition which heat-treated high temperature further from the condition. By heat-treatment of high temperature, it is the above (d). It became the silicide layer 11 in which the produced silicide layer 10 reacted to with the silicon substrate 6 further, and thickness increased.

[0038] [Example of a comparison] N+ of the device used as a sample It is As to a diffusion layer field 50keV(s) and 3E15/cm 2 It is conditions and is P+. He is BF2 to a diffusion layer field. 30keV(s) and 2E15cm2 After pouring in on conditions, it is RTA for 10 seconds at 1000 degrees C. Annealing was performed. Then, 20keV and 3E14/cm 2 As was poured in on the surface of the silicon substrate on conditions. This process is an approach by the conventional technique which makes Si amorphous.

[0039] Then, HF water solution removed the natural oxidation film of a silicon substrate surface.

Subsequently it is TiN in 80A of thickness about Co. By thickness 200 **, membranes are formed by the continuation spatter in a vacuum in this order, respectively, and it is RTA. 570 degrees C and annealing for 60 seconds which were used were performed in nitrogen-gas-atmosphere mind. Subsequently, a sulfuric-acid:filtered water = Co and TiN unreacted with the solution of 4:1 It removed. At this time, the thickness of silicide was about 150 **. Then, it is RTA about annealing for 30 seconds at 750 **. It was used and carried out in nitrogen-gas-atmosphere mind. The final thickness of a silicide layer was about 300 **.

[0040] Average junction leakage current was 1.8V, and the samples in which the silicide layer was formed by the conventional approach were 1.8E-8A/cm2 (N+ diffusion layer side) and 3.4E-7A/cm2 (P+ diffusion layer side). On the other hand, average junction leakage current was 1.8V, and the samples in which silicide was formed with the application of the manufacture approach of the semiconductor device of this invention shown in said example were 1.8E-8A/cm2 (N+ diffusion layer side) and 2.5E-8A/cm2 (P+ diffusion layer side). Leakage current is 1 although the junction to a part for the joint under an N+/P+ diffusion layer is not destroyed in the sample devices in which the silicide layer was formed by the conventional approach. It increased double figures from the digit.

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* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Outline process drawing explaining the gestalt of implementation of the manufacture approach of the semiconductor device by this invention.
[Drawing 2] Outline process drawing explaining the gestalt of implementation of the manufacture approach of the semiconductor device by the conventional technique.
[Description of Notations]
1 Gate Electrode
2 Sidewall
3 Shallow Diffusion Layer
4 Component Isolation Region
5 Amorphous Layer
6 Silicon Substrate (Silicon Layer)
7 Deep Diffusion Layer
8 Metal Membrane
9 Antioxidizing Film
10 Silicide Layer
11 Silicide Layer of Low Resistance

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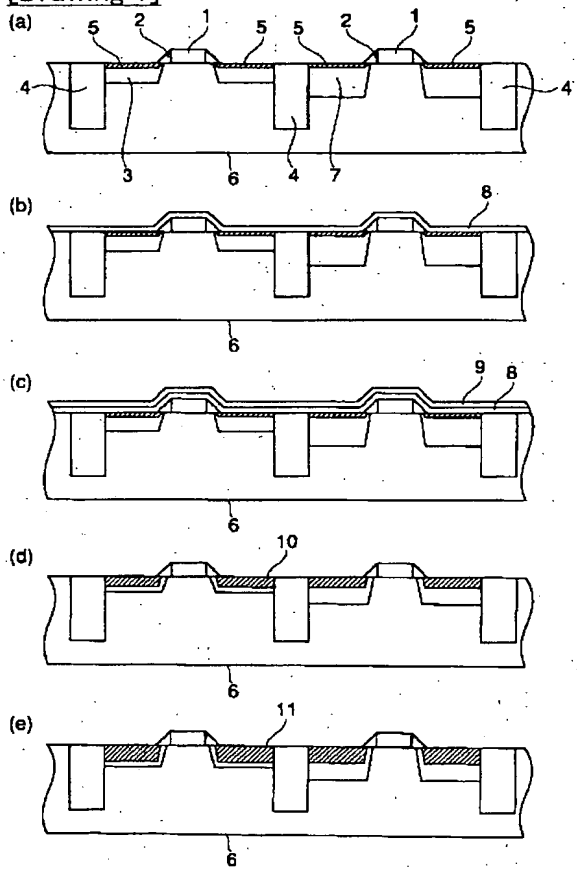
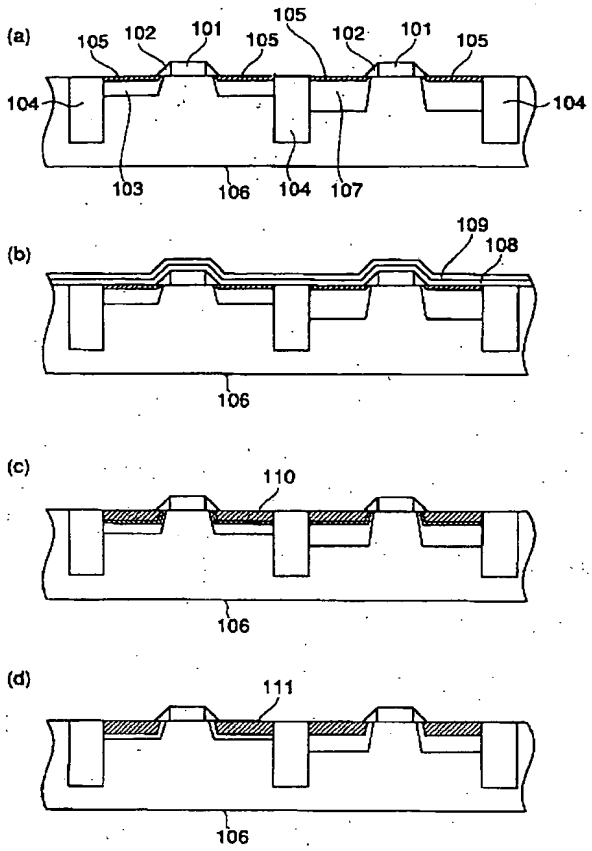
DRAWINGS

[Drawing 1]



[Drawing 2]



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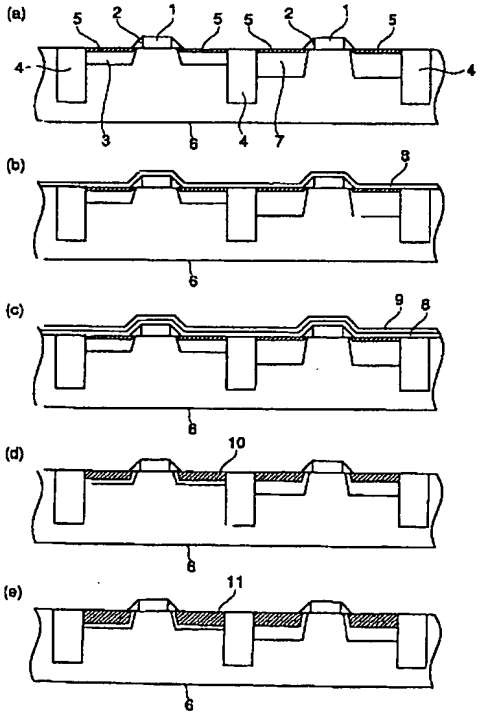
最終頁に続く

(54)【発明の名称】　半導体装置の製造方法

(57)【要約】
【課題】　より均一で接合リーク等の欠陥を生じにくいシリサイド層を半導体装置に形成する。
【解決手段】　シリコン層の表面に金属膜を形成し、次いで、このシリコン層を加熱して金属膜とシリコン層とを反応させ、シリコン層の表面にシリサイド層に形成するに際し、金属膜の形成時にシリコン層の表面を加熱する前加熱工程を含むことを特徴とする半導体装置の製造方法を提供する。



【特許請求の範囲】
【請求項１】　シリコン層の表面に、第１の加熱を行い、その状態で金属膜を積層し、次いで、第２の加熱を行ってシリコン層の少なくとも表面層をシリサイド化することを特徴とする半導体装置の製造方法。
【請求項２】　第１の加熱温度が３００～４００℃である請求項１に記載の半導体装置の製造方法。
【請求項３】　第２の加熱温度が５００～９００℃である請求項１に記載の半導体装置の製造方法。
【請求項４】　金属膜が形成された後、シリコン層の表面の温度を第１の加熱温度から一旦降下させた状態で、金属膜の表面に酸化防止膜を形成し、次いで、第２の加熱を行う請求項１から３のいずれか１つに記載の半導体装置の製造方法。
【請求項５】　第１の加熱温度からシリコン層の表面の温度を２００℃以下に一旦降下させた状態で、金属膜の表面に酸化防止膜を形成する請求項４に記載の半導体装置の製造方法。
【請求項６】　第１の加熱を行う前に、シリコン層の表面から深さ１２ｎｍまでの領域の一部または全部をアモルファス化させる工程を含む請求項１から５のいずれか１つに記載の半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は半導体装置の製造方法に関し、さらに詳しくは、シリコン層の少なくとも表面層をシリサイド化する半導体装置の製造方法に関する。
【０００２】
【従来の技術】半導体デバイスの製造において、デバイスサイズの微細化が進められている。これは微細化が進むほど１枚の基板上から取れるデバイス数が多くなり、半導体デバイスがトランジスタを含むような場合にはトランジスタの特性の向上につながるためである。しかし、微細化の進展と共にトランジスタそのものではなく、配線部分の抵抗がトランジスタの動作速度に影響を与えるようになってきた。このため、半導体デバイスの製造においては、ゲートラインあるいは拡散領域等の抵抗を下げるためのサリサイド技術が必須となっている。
【０００３】サリサイド技術を用いた半導体デバイスの製造では、まず、シリコン基板に通常のトランジスタ作製を行う。すなわち、素子分離領域、ウエル、ゲートおよびN+／P+拡散層の形成である。次に、上記のトランジスタ形成工程を終了したシリコン基板に対して弗化水素酸水溶液等を用いて表面処理を施してシリコン表面を露出させた後に、シリコン表面に金属膜を成膜する。
【０００４】次いで、この金属膜の上に前記金属膜の酸化を防止するための保護膜を設け、さらに、RTA 処理（Rapid Thermal Annealling）等によって基板を加熱し（シリサイドを形成するためのアニール）、基板のシリコンと前記金属膜とを反応させることによって基板上にシリサイド層を形成する。シリサイド層が形成されたシリコン基板の表面上には、酸化膜により形成された素子分離領域あるいはサイドウォール等のシリサイド反応を起こさない部分が存在する。
【０００５】これらの部分は電気的分離のための部分であるため、この上に未反応の金属が残っていては問題がある。そこで、素子分離領域やサイドウォール上の未反応の金属膜を除去する薬剤処理を行う。この処理には、シリコン基板の表面に形成された前記金属膜を溶解し、かつシリサイドを溶解しない薬液が用いられる。
【０００６】最後に、前記のシリサイドを形成するためのアニールにおける加熱温度より高い温度で、シリサイドの相変化のためのアニールを行い、シリサイド層をより抵抗の低い構造に変化させる。アニール処理を２回に分ける理由は、シリサイドを形成するためのアニールで温度を上げ過ぎると、基板のシリコンが素子分離領域やサイドウォール上の金属膜中へ激しく拡散し、シリサイドが素子分離領域やサイドウォール上にも形成されるためである。このようなサリサイド技術を用いることにより、従来のフォトリソグラフィー技術を使わずに、反応の選択性を利用することによってシリコン表面のみに低抵抗の導電領域を作製できる。
【０００７】しかし、上記のサリサイド技術を用いた方法の欠点は、シリサイドの形成の際に基板のシリコンを消費することである。微細化の進行に伴ってN+／P+拡散層の厚さがより薄くなっている上に、シリサイド層の形成のためにこの領域のシリコンが消費されると、形成されたシリサイド層の下面とN+／P+拡散層の下の接合部分との距離がさらに接近し、接合リークが生じやすくなる。この場合、シリサイド層を薄くすれば、シリサイドの形成時のシリコンの消費を抑え、前記接合部分とシリサイド層の底面との距離が大きくなって接合リークを減らすことができるが、必然的にゲートラインや拡散領域のシート抵抗の上昇を招く。
【０００８】通常、接合リークおよびシート抵抗の上昇を抑えるための対策として、シリサイドを平坦に形成する手法が用いられる。シリサイドの平坦性は、基板のシリコン表面の状態に基づいて上記のような金属とシリコンの反応時に大きく変化することが知られている。これは、前処理等により基板のシリコンの表面から酸化膜を取り除いても金属膜を成膜するまでの間に、シリコン表面が大気に曝されて再び酸化膜が生じるためである。
【０００９】金属膜と基板シリコンの間に生じた酸化膜が極めて薄い場合であれば、シリサイドは形成される。これは通常、シリサイドの形成に用いられる金属には、シリコン酸化膜に対する還元性があるためである。しかしながら、シリコン基板の表面に生じる酸化膜は、通常、不均一であるため、シリサイドが生じやすい部分と生じにくい部分が形成され、結果として不均一なシリサ

イド層がシリコン基板上に形成される。不均一な酸化膜の上に形成されたシリサイド層は、その厚みが厚い部分においてシリサイド層の底面とN+／P+拡散層の下の接合部分との距離が接近するために接合リークを起こしやすく、さらに、シリサイド層自体の平均膜厚が薄いためにシート抵抗が大きい。

【００１０】また、デバイスによっては、その作製工程の途中でシリコン表面にカーボン、フッ素等が混入することがある。これらは、主にゲートエッチングやサイドウォール形成時のエッチバック等の工程において生じやすい。このような元素の混入はシリコン表面の不均一性を増大させ、前記した酸化膜による不均一性と同様の作用によって、接合リークを生じさせると考えられる。

【００１１】このようなシリサイドの不均一性を改善し、接合リークを防止する方法として、例えば、特開平9－251967号公報に記載された半導体装置の製造方法がある。上記公報に記載された製造方法を図２を参照しながら工程順に説明する。なお、この図は説明のために部分的に縮尺を拡大した概略図であるため、その形状あるいは大きさは必ずしも現実のデバイスと同じではない。

【００１２】図２の(a) は、トランジスタの形成を終了した後、シリコン表面をアモルファス化した状態である。１０１はゲート、１０２はサイドウォール、１０３は浅い拡散層、１０４は素子分離領域、１０５はイオンの注入によって形成されたアモルファス領域、１０７は深い拡散層、１０６は基板としてのシリコン（シリコンウエハ）である。説明を簡略化するために、ゲート酸化膜、ウエル等は図中において省略している。

【００１３】図２の(b) は金属膜１０８および酸化防止膜１０９の形成を終了した状態である。金属膜１０８には、コバルトがよく用いられ、コバルトがシリコン１０６と反応してシリサイドを生じさせる。酸化防止膜１０９には、窒化チタンがよく用いられ、金属膜１０８の酸化を防止する膜として機能する。

【００１４】図２の(c) は前記の(b) の状態で、シリサイドを形成するアニールを行った後の状態である。シリサイド層１１０は、前記の(a) において設けられたアモルファス領域１０５内に収まるように形成される。均一にアモルファス化したアモルファス領域１０５内のシリコンと金属膜１０９のコバルトが反応するため、形成されたシリサイド層１１０は平坦性が高い。図２の(d) は(c) の状態で、シリサイドの相変化のためのアニールを行った後の状態である。シリサイドの相変化のためのアニールは、シリサイドを形成するアニールよりも高温で行われる。このアニール処理により、(c) で生じたシリサイド層１１０がさらに基板のシリコン１０６と反応し、膜厚が増大したシリサイド層１１１を形成する。なお、前記の(c) において均一なシリサイド層１１０が生じるため、この状態でも、ＰＮ接合部とシリサイド層１１０の距離が最も近い部分においても接合リークを生じない程度の距離が保たれる。

【００１５】

【発明が解決しようとする課題】前記したように、イオンを注入してシリコン表面のアモルファス化を行うためには、通常、質量が比較的大きい砒素等のイオンが用いられる。しかし、このようなイオンは、アモルファス層を形成しやすい反面、イオンが注入された領域よりも深い領域に欠陥を生じやすいことが知られている。このような欠陥が生じると、シリコンの接合リークの原因となる準位を生じやすい。リーク電流の増大は、素子の待機時の消費電流を増大し、特に電池などにより動作する携帯機器用のLSI においては重大な問題となる。

【００１６】この発明は上記問題点に鑑みてなされたものであり、より均一で接合リーク等の欠陥を生じにくいシリサイド層を半導体装置に形成することを目的とする。

【００１７】

【課題を解決するための手段】この発明によれば、シリコン層の表面に、第１の加熱を行い、その状態で金属膜を積層し、次いで、第２の加熱を行ってシリコン層の少なくとも表面層をシリサイド化することを特徴とする半導体装置の製造方法が提供される。

【００１８】すなわち、この発明では、昇温されたシリコン層の表面が有する熱エネルギーを利用して、シリコン層の表面に形成されている酸化膜と金属膜を形成するためにシリコン層の表面に供給された金属原子とを反応させ、前記酸化膜を還元する。これによって、前記酸化膜は消滅あるいは薄膜化するので、シリコン層の表面に均一で平坦なシリサイド層を形成することができる。

【００１９】この発明におけるシリコン層としては、キャパシタ、トランジスタ等の半導体素子の回路部が形成されるようなシリコン基板自体でもよいし、これらの素子の導電層あるいは配線層として機能するシリコン層でもよい。

【００２０】第１の加熱温度は３００～４００℃が好ましい。第１の加熱温度が３００℃より低いと、シリコンとシリサイド層の界面に凹凸が生じやすい。第１の加熱温度が４００℃より高いと、金属膜のスパッタ中にプラズマダメージによりゲート酸化膜等の耐圧劣化が生じやすい。

【００２１】この発明における金属膜の材料としては、コバルト、チタン等の高融点金属が挙げられるが、シリコンと反応してシリサイドを形成する金属であれば、特に限定されない。金属膜の形成方法としては、蒸着法、ＣＶＤ法およびスパッタ等の従来の薄膜形成技術を用いることができる。

【００２２】この発明における第２の加熱の手段としては、炉アニール、ＲＴＡ等によるアニールが挙げられる。第２の加熱温度は５００～９００℃が好ましい。

【００２３】この発明には、金属膜が形成された後、シ

リコン層の表面の温度を第１の加熱温度から一旦降下させた状態で、金属膜の表面に酸化防止膜を形成し、次いで、第２の加熱を行う工程が含まれる。すなわち、この発明の第１の加熱工程を含む製造方法を用いてトランジスタを構成するシリコン層をシリサイド化する場合には、ゲート酸化膜の耐圧を劣化させることがあるが、上記の冷却によって、金属膜の成膜中に酸化膜内を流れる電流量を減らすことができるので、前記の耐圧の劣化が防止される。酸化防止膜形成時のシリコン層の温度は、２００℃以下に降下していればよく、下限は特に定めることはなく、室温付近まで冷却してもよい。この発明における酸化防止膜の材料としては、窒化チタンが挙げられるが、従来の酸化防止膜の材料であれば、特に限定されない。酸化防止膜の形成方法としては、蒸着法、ＣＶＤ法およびスパッタ等の従来の薄膜形成技術を用いることができる。この発明では、金属膜の形成に用いた成膜装置で酸化防止膜の形成を連続して行うことができるので、金属膜の酸化を防止することができる。

【００２４】上記の方法を用いた上で、さらなる接合リークの改善を所望する場合には、第１の加熱を行う前に、シリコン層の表面から深さ１２ｎｍまでの領域の一部または全部をアモルファス化させることが好ましい。すなわち、シリコン層の表面がカーボンやフッ素等により汚染されているために、シリコン層の温度を高くして金属を成膜しても、形成されるシリサイドが不均一になってしまう場合は、シリコン層の最表面をアモルファス化することにより、カーボンやフッ素とシリコンの結合が切断され前記金属との反応が促進される。これにより前記金属とシリコンの反応が均一に進むようになり、シリサイドが均一に形成され接合リークが抑制される。上記のアモルファス化は、通常、シリコン層の上層部に浅い部分のみにイオン種が拡散し、シリコン層の深い部分にイオン種が侵入しないように行われるのが好ましい。

【００２５】イオン種の侵入深さは、主に注入エネルギーに依存する。上記の浅いイオン注入に用いられるイオン種としては、ホウ素、燐、砒素、窒素、珪素等が挙げられる。これらの中でも、比較的重い砒素が好ましい。この発明におけるイオン注入量は１Ｅ１４～８Ｅ１４/cm^{2}オーダー、イオン注入エネルギーは５～１５keV が例示されるが、これらは目的に応じて適宜調整される。

【００２６】上記のように、この発明におけるイオン注入エネルギーは、従来に比べて小さいために、注入されたイオン種によって欠陥を生じる領域がシリコン層に発生しても、その深さがあまり深くないため、接合領域に影響を及ぼさない。

【００２７】この発明では、シリコン層の表面が露出していない状態で（例えば、シリコン表面に存在する酸化膜等を除去しないままの状態で、あるいは保護膜を積層した状態で）、イオン注入を行い、結果としてシリコン層の深い部分へのイオン種の侵入を止め、シリコン層の上層部の浅い部分のみにイオン種を注入することができる。したがって、イオン注入装置の能力に係わりなく浅いイオン注入が可能になる。

【００２８】

【発明の実施の形態】以下、図面に基づいてこの発明の半導体装置の製造方法の実施の形態を説明するが、これらによってこの発明は限定されるものではない。図１は、この発明によるＭＯＳ型トランジスタの製造工程の概略を示す。なお、図１は説明のために部分的に縮尺を拡大しているので、必ずしも現実のデバイスの形状とは同じではない。また、簡略化のために図中からゲート酸化膜、ウエル等は省略している。

【００２９】実施例

図１を参照しながら、本発明の実施例を説明する。図１の(a) はＭＯＳ型トランジスタの形成を終了した後、シリコン表面をアモルファス化した状態を示す。１はゲート電極、２はサイドウォール、３は浅い拡散層、４は素子分離領域、５はアモルファス層、７は深い拡散層、６はシリコン基板（シリコンウエハ）である。

【００３０】アモルファス層の形成はシリサイド化するシリコン基板６の表面にカーボン、フッ素等の汚染が生じている場合に行う。浅い拡散層３の深さは１２０ｎｍ、深い拡散層７の深さは１６０ｎｍである。拡散層３、７のそれぞれは、BF_2 およびAsの注入により作製されている。

【００３１】サイドウォール２の形成は、シリコン基板６の表面までエッチバックする方法およびシリコン６の表面に１０ｎｍ程度の酸化膜を残す方法がある。後者の方法によれば、シリコン基板６の表面に生じるエッチングの影響によるカーボンやフッ素の汚染を減らすことができるが、複数のデバイスを同一プロセスで作製する場合等では、エッチバックすべき膜厚が部分によって異なる場合もあり、シリコン６の表面に酸化膜を残すことが難しい場合もある。

【００３２】アモルファス層５の形成は砒素イオンの注入により行った。通常、砒素イオンをシリコン基板６に注入すると、平均投影飛程よりもシリコン基板６の表面側にアモルファス領域を生じる。さらに平均投影飛程よりも深い部分では、注入されたAsによって叩き出されたSi原子が入り込んだ領域を生じる。こうした領域には欠陥ができやすく、さらに加熱工程によって転位を生じる。これらが接合リークを生じる原因となる。

【００３３】しかしながら、本発明においてはシリコン基板６の表面の極浅い領域に砒素イオンを注入するため、注入エネルギーは10keV 、注入イオン量（ドープ量）は3E14/cm2）である。このように、注入エネルギーが小さいために、上記したように注入された砒素イオンによって叩き出されたシリコン原子が入り込んだ領域が生じても、その深さがあまり深くないため、接合領域に影響を及ぼさない。

【００３４】図１の(b) は第１の加熱後、金属膜８の形成を終了した状態である。金属膜８は、シリコン基板６と反応してシリサイドを生じさせるための金属膜であり、この例においてはコバルトを用いた。金属膜８の成膜はスパッタにより行った。スパッタ装置の電力を５００W 、装置内の圧力を５mT 程度とした。スパッタ時のシリコン基板６の温度（第１の加熱温度）は、３５０℃とした。なお、第１の加熱温度が３００℃以下では、シリサイドとシリコンの界面に凹凸が生じ、それによって接合リークを生じやすい。接合リークを減らすために凹凸はそのままにして金属膜８を薄くするとシート抵抗が高くなる。第１の加熱温度が４００℃以上では、スパッタ中にプラズマダメージによりゲート酸化膜が耐圧劣化を生じる。

【００３５】図１の(c) は金属膜８の形成終了後、シリコン基板６の温度を一旦降下させ、その状態で酸化防止膜９の形成を行った状態である。酸化防止膜９はこの例においては窒化チタンを用い、スパッタにより成膜した。スパッタ装置の電力を２kW 、装置内の圧力を１０mT 程度とした。金属膜８のスパッタと酸化防止膜９のスパッタは同一のスパッタ装置内で真空を維持したまま連続で行った。これは金属膜８のコバルトの酸化を防ぐためである。なお、スパッタ開始時のシリコン基板６の温度は、７０℃であった。

【００３６】酸化防止膜９のスパッタ時にシリコン基板６の温度が２００℃を超えると、酸化防止膜９のスパッタ時のプラズマのダメージにより、ゲート絶縁膜の耐圧が劣化する場合がある。耐圧の劣化の度合いはデバイスによって異なる。ゲート絶縁膜の耐圧の劣化が確認された場合は、金属膜８のスパッタ後に同一装置内において、１０E －８オーダーの真空を維持した状態でシリコン基板６を保持しながらシリコン基板６の温度を２００℃まで下げた。しかし、基板温度を２００℃まで下げるために処理時間が長くなり、スループットは低下する。

【００３７】図１の(d) は酸化防止膜９の形成を終了した後、第２の加熱処理を行った後の状態である。拡散層３、７には、シリサイド層１０がそれぞれ形成される。第２の加熱温度は、５７０℃であった。図１の (e)は上記(d) の状態からさらに高温度の加熱処理を行った状態である。高温度の加熱処理により、上記(d) で生じたシリサイド層１０がさらにシリコン基板６と反応して膜厚が増大したシリサイド層１１となった。

【００３８】〔比較例〕試料となるデバイスのN^+ 拡散層領域にAsを50keV 、3E15/cm^2 の条件で、また、P^+ 拡散層領域にBF^2 を30keV 、2E15cm^2 の条件で注入した後に1000℃で10秒間のRTA アニールを行った。その後、20keV 、3E14/cm^2 の条件でシリコン基板の表面にAsを注入した。この工程は、Siをアモルファス化する従来技術による方法である。

【００３９】その後、HF水溶液によりシリコン基板表面の自然酸化膜を除去した。Coを膜厚80Åで、次いで、TiN を膜厚200 Åで、この順にそれぞれ真空中で連続スパッタにより成膜し、RTA を使用した５７０℃、６０秒間のアニールを窒素雰囲気中で行った。次いで、硫酸：過水＝４：１の溶液で未反応のCoとTiN を除去した。この時点でシリサイドの膜厚は約150 Åであった。その後、750 ℃で30秒間のアニールをRTA を使用して窒素雰囲気中で行った。シリサイド層の最終的な厚さは約300 Åであった。

【００４０】従来方法によりシリサイド層が形成された試料は、平均接合リーク電流が、1.8Vで、1.8E-8Å/cm^2 （N^+ 拡散層側）および3.4E-7Å/cm^2 （P^+ 拡散層側）であった。これに対し、前記実施例で示した本発明の半導体装置の製造方法を適用してシリサイドが形成された試料は、平均接合リーク電流が、1.8Vで、1.8E-8Å/cm^2 （N^+ 拡散層側）および2.5E-8Å/cm^2 （P^+ 拡散層側）であった。従来方法によりシリサイド層が形成された試料デバイスでは、N+／P+拡散層の下の接合部分との接合は破壊されないものの、リーク電流が1 桁から２桁増大した。

【００４１】

【発明の効果】この発明では、昇温されたシリコン層の表面が有する熱エネルギーを利用して、シリコン層の表面に形成されている酸化膜と金属膜を形成するためにシリコン層の表面に供給された金属原子とを反応させ、前記酸化膜を還元する。これによって、前記酸化膜は消滅あるいは薄膜化するので、シリコン層の表面に均一で平坦なシリサイド層を形成することができる。したがって、半導体装置における接合リークが生じにくくなる。また、金属膜を形成した後、シリコン層の温度を一旦降下させた状態で酸化防止膜を形成することにより、シリコン層に形成される半導体装置における耐圧の劣化が防止される。

【００４２】シリコン層の表面をアモルファス化することにより、カーボンやフッ素とシリコンの結合が切断され、金属膜を形成する金属原子とシリコンの反応が促進される。これにより、金属膜とシリコンの反応が均一に進み、シリサイドが均一に形成されて接合リークが抑制される。

【図面の簡単な説明】

【図１】この発明による半導体装置の製造方法の実施の形態を説明する概略工程図。

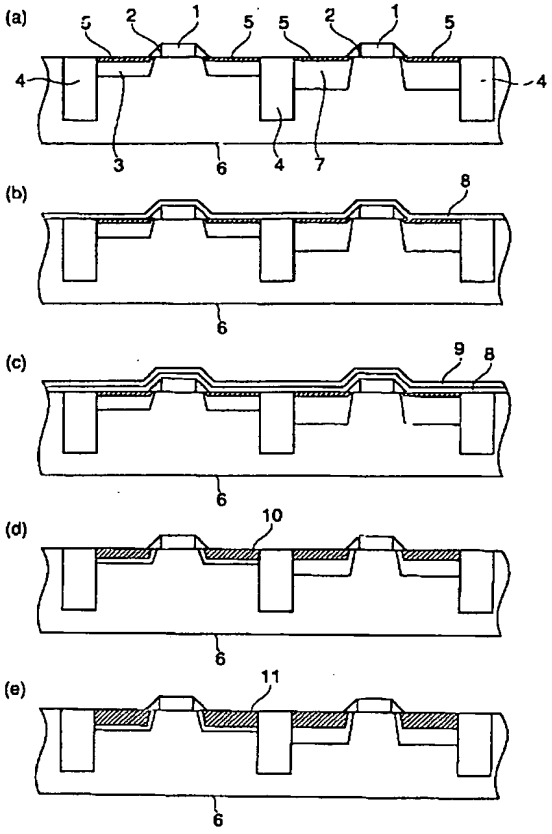
【図２】従来技術による半導体装置の製造方法の実施の形態を説明する概略工程図。

【符号の説明】

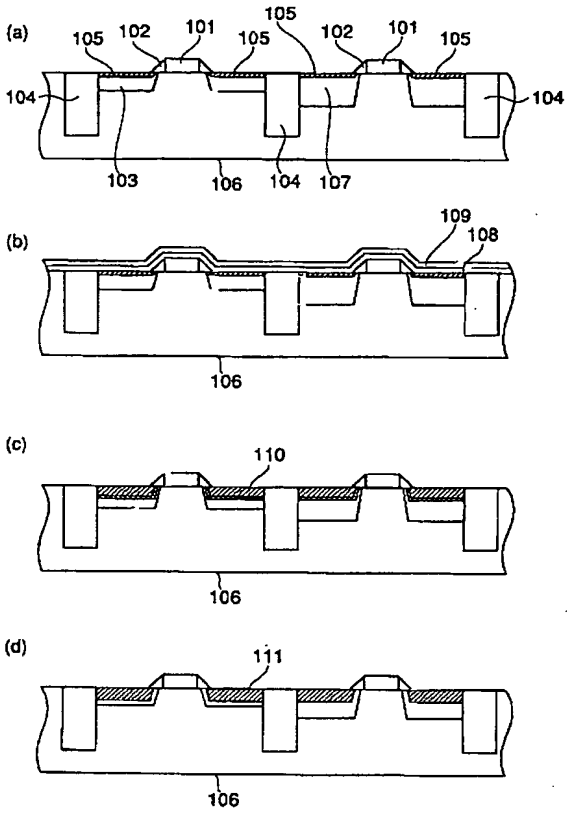
１　ゲート電極
２　サイドウォール
３　浅い拡散層
４　素子分離領域
５　アモルファス層

6　シリコン基板（シリコン層）
7　深い拡散層
8　金属膜
9　酸化防止膜
10　シリサイド層
11　低抵抗のシリサイド層

【図1】



【図2】



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